CLAIMS

What is claimed is:

1   1.   A system comprising:

2   a central processing unit (CPU);

3   one or more cache memories, coupled to the CPU, each to store only data

4   for loads to be processed by the CPU that have a vitality matching the latency

5   associated with the respective cache memory;

1   2.   The system of claim 1 wherein the one or more cache memories comprise:

2   a first cache memory, coupled to the CPU, to store only data for vital loads

3   that are to be immediately processed at the CPU; and

4   a second cache memory, coupled to the CPU and the first cache, to store

5   non-vital loads to be processed at the CPU.

1   3.   The system of claim 2 wherein the one or more cache memories further

2   comprise a third cache memory, coupled to the CPU and the second cache

3   memory, to store data for semi-vital loads to be processed at the CPU.

1   4.   The system of claim 3 wherein the CPU accesses to the first cache

2   memory, the second cache memory and the third cache memory in parallel.

1   5.   The system of claim 3 wherein vital loads are directly assigned to the first

2   cache memory, semi-vital loads are directly assigned to the third cache memory

3   and non-vital loads are directly assigned to the second cache memory.

1   6.   The system of claim 5 wherein the assignment of the loads to the

2   respective caches is performed statically.

1   7.   The system of claim 6 wherein the assignment of the loads is performed at

2   a compiler.

1   8.   The system of claim 3 wherein vital loads are to be processed at the CPU

2   within one clock cycle.

1   9.   The system of claim 8 wherein semi-vital loads are to be processed at the

2   CPU within three clock cycles.

1   10.   The system of claim 9 wherein non-vital loads are not to be processed at

2   the CPU for at least four clock cycles.

1   11.   The system of claim 3 wherein the first cache memory is a 265B cache and

2   the third cache memory is a 1KB cache.

1   12.   The system of claim 11 wherein the second cache memory is physically

2   larger than the third cache memory.

1   13.   The system of claim 3 wherein the first cache memory and the third cache

2   memory operate at the same level in cache hierarchy.

1 14. The system of claim 3 wherein vital loads update the first cache memory

2 and the second cache memory.

1 15. The system of claim 14 wherein semi-vital loads update the third cache

2 memory and the second cache memory.

1 16. The system of claim 15 wherein non-vital loads update the second cache

2 memory.

3 17. A method comprising:

4   identifying load instructions having a first vitality level by filtering out

5 load instructions having a dependence distance greater than a predetermined

6 clock cycle;

7   identifying load instructions having a second vitality level;

8   assigning load instructions having the first vitality level to be stored in a

9 first cache memory; and

10   assigning load instructions having the second vitality level in a second

11 cache memory.

1 18. The method of claim 17 further comprising:

2   identifying load instructions having a third vitality level after identifying

3 load instructions having the first vitality level; and

4   assigning load instructions having the third vitality level to be stored in a

5   third cache memory.

1   19.   The method of claim 18 further comprising performing a profile, after

2   identifying the load instructions having the first vitality level, to identify the

3   remaining load instructions that frequently miss in the first cache memory and

4   lines that are not used.

1   20.   The method of claim 18 further comprising performing a profile, after

2   identifying the load instructions having the third vitality level, to identify the

3   remaining load instructions that frequently miss in the third cache memory and

4   lines that are not used.

1   21.   A computer system comprising:

2   a central processing unit (CPU);

3   a first cache memory, coupled to the CPU, to store only data for vital loads

4   that are to be immediately processed at the CPU;

5   a second cache memory, coupled to the CPU, to store data for semi-vital

6   loads to be processed at the CPU

7   a third cache memory, coupled to the CPU the first cache memory and the

8   second cache memory, to store non-vital loads to be processed at the CPU;

9   a chipset coupled to the CPU; and

10   a main memory device coupled to the chipset.

1   22.   The system of claim 21 wherein the CPU accesses to the first cache

2   memory, the second cache memory and the third cache memory in parallel.

1   23.   The system of claim 22 wherein vital loads are directly assigned to the first

2   cache memory, semi-vital loads are directly assigned to the second cache

3   memory and non-vital loads are directly assigned to the third cache memory.

1   24.   The system of claim 23 wherein vital loads are to be processed at the CPU

2   within one clock cycle, the semi-vital loads are to be processed at the CPU within

3   three clock cycles and non-vital loads are not to be processed at the CPU for at

4   least four clock cycles.

1   25.   The system of claim 23 wherein the first cache memory and the second

2   cache memory operate at the same level in cache hierarchy.

1   26.   The system of claim 23 wherein vital loads update the first cache memory

2   and the third cache memory.

1   27.   The system of claim 26 wherein semi-vital loads update the second cache

2   memory and the third cache memory.

1   28.   The system of claim 27 wherein non-vital loads update the third cache

2   memory.